International Journal of Electronics and Communication Engineering (IJECE)
ISSN 2278-9901
Vol. 2, Issue 3, July 2013, 97-102

International Academy of Science, Engineering and Technology
Connecting Researchers; Nurturing Innovations

REVIEW OF FULL ADDER USING REVERSIBLE LOGIC

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ABSTRACT

In the field of cryptography, optical information processing low power CMOS design and nanotechnology Reversible logic has found its applications and has become one of the promising research directions This paper presents a novel and quantum cost efficient reversible full adder gate in nanotechnology. This gate can work singly as a reversible full adder unit and requires only one clock cycle. The proposed gate is a universal gate in the sense that it can be used to synthesize any arbitrary Boolean functions. It has been demonstrated that the hardware complexity offered by the proposed gate is less than the existing counterparts. The proposed reversible full adder is then compared with the adder and the floating point adder.

KEYWORDS: Component, Floating Point Adder, Reversible Logic

INTRODUCTION

Power dissipation is one of the most important factors in VLSI circuit design. Irreversible logic circuits dissipates kT*log 2 Joule (k is the Boltzmann constant and T is the absolute temperature) heat for every bit of information that is lost irrespective of their implementation technologies [1]. Information is lost when the input vectors cannot be recovered from circuit's output vectors. Reversible logic naturally takes care of heating since in reversible circuits the input vectors can be uniquely recovered from its corresponding output vectors. Bennett [2] showed that zero energy dissipation is possible only if the gating network consists of reversible gates. Thus reversibility will become future trends towards low power dissipating circuit design.

Reversible logic design differs significantly from traditional combinational logic design approaches. In reversible logic circuit the number of input lines must be equal the number of output lines, each output will be used only once and the resulting circuit must be acyclic [3]. The output lines that are not used further are termed as garbage outputs. One of the most challenging tasks is to reduce these garbages [3]. Any reversible logic gate realizes only the functions that are reversible.

But many of the Boolean functions are not reversible. Before realizing these functions, we need to transform those irreversible functions into reversible one. Any transformation algorithm that converts an irreversible function to a reversible one introduces input lines that are set to zero in the circuit's input side [4-5]. These inputs are termed as constant inputs. Therefore, any efficient 0.....reversible logic design should minimize the garbages as well as constant inputs.

This paper presents a novel 4*4 reversible gate namely Peres Full Adder Gate (PFAG) , that is, it has 4-input lines and 4-output lines. This gate can be used to realize any arbitrary Boolean function and therefore universal. The hardware complexity of this gate is less compared to the existing ones and requires only one clock cycle. The quantum realization cost of this gate is only 8 and ready for use in

Table 1

A	B	P
0	0	0
0	1	1
1	0	1
1	1	0

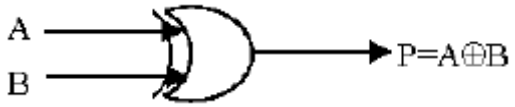

Figure 1: Irreversible EX-OR Gate

Garbage Output

A	B	P	Q
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

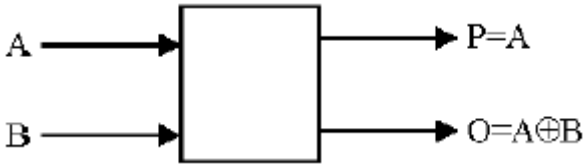

Figure 2: Reversible EX-OR Gate

REVERSIBLE LOGIC GATES

There exist many reversible gates in the literature. Among them 2*2 Feynman gate [6] (shown in figure 3), 3*3 Fredkin gate [7] (shown in figure 4), 3*3 Toffoli gate [8] (shown in figure 5) and 3*3 Peres gate [9] (shown in figure 6) is the most referred. The detailed cost of a reversible gate depends on any particular realization of quantum logic. Generally, the cost is calculated as a total sum of 2*2 quantum primitives used. The cost of Toffoli gate is exactly the same as the cost of Fredkin gate and is 5. The only cheapest quantum realization of a complete (universal) 3*3 reversible gate is Peres gate and its cost is 4.

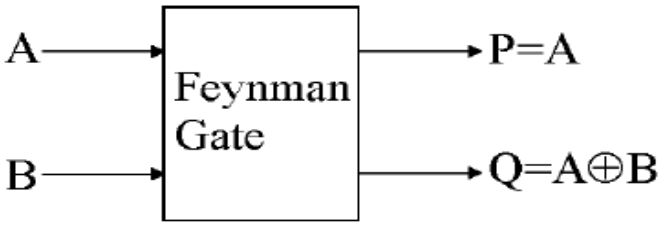

Figure 3: 2*2 Feynman Gate

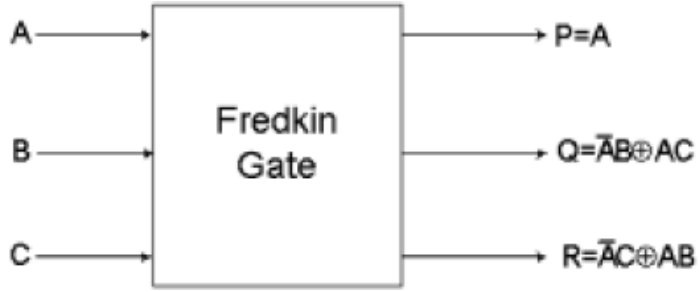

Figure 4: 3*3 Fredkin Gate

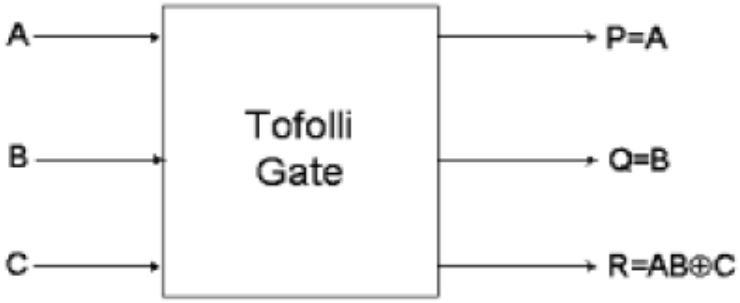

Figure 5: 3*3 Tofolli Gate

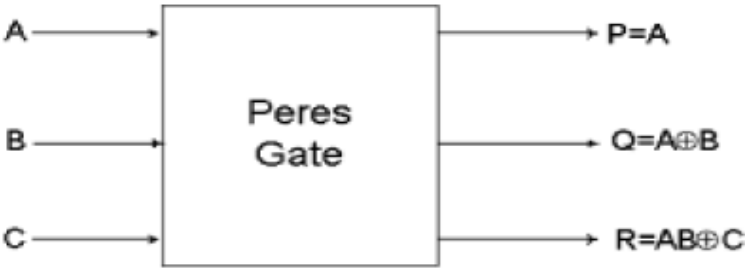

Figure 6: 3*3 Peres Gate

REVERSIBLE LOGIC IMPLEMENTATION OF FULL ADDER CIRCUIT

Full adder is the fundamental building block in many computational units. The anticipated paradigm shift logic compatible with optical and quantum requires compatible reversible adder implementations. The full adder circuit's output is given by the following equations:

$$Sum = A \oplus B \oplus C_{in}$$

$$C_{out} = (A \oplus B)\, C_{in} \oplus AB$$

The reversible logic implementation of full-adder circuit and other adder circuits and their minimization issues has been discussed in [10-13]. It has been shown in [11] and [13] that any reversible logic realization of full adder circuit includes at least two garbage outputs and one constant input. The author in [10-13] has given a quantum cost efficient reversible full adder circuit that is realized using two 3*3 Peres gates only (shown in figure 6). This implementation of reversible full adder circuit is also efficient in terms of gate count, garbage outputs and constant input than the existing counter parts.

For this implementation, I will be using the Peres gate as it is the gate with the lower quantum cost as can be seen in the figures 7. The Peres' implemented Full Adder with its corresponding quantum cost can be seen below:

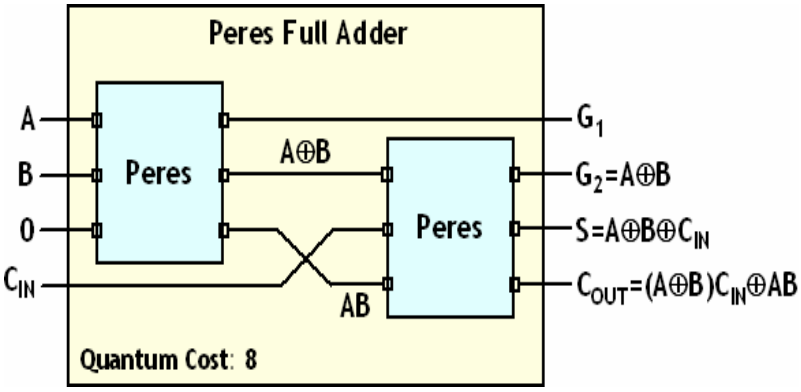

Figure 7: Peres Full Adder

This PFA (Peres Full Adder) can be taken as a block in order to facilitate the notation of its expansion. The inputs order was also changed to better fit in an expansion diagram.

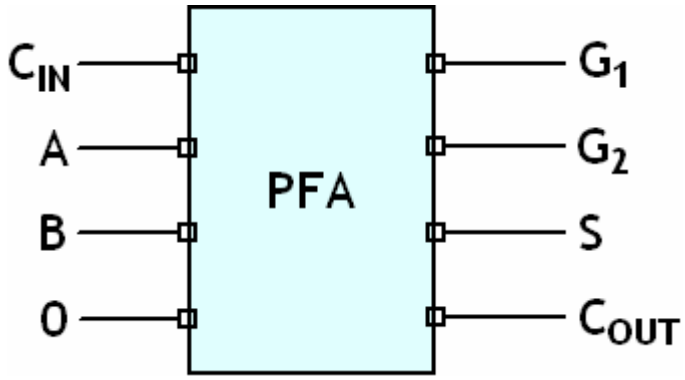

Figure 8: PFA as a Block

Once we take the PFA as a block, we can derive the algorithm to implement an n-bits adder. This algorithm was implemented in this design and can be seen in figure 9.

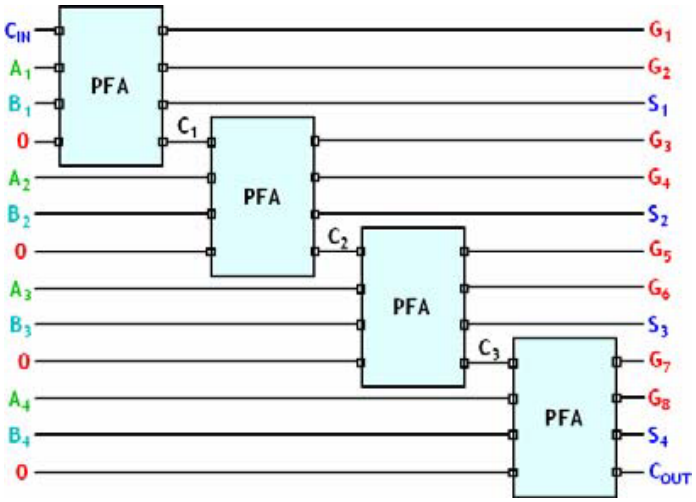

Figure 9: 4-bits Adder Implementation

INPUTS

The inputs of the complete 4 bits adder are three input vectors (4 bits) and a single bit Cin (Carry in). Two of the three input vectors are the desired added 4-bits values. The remaining vector could be called the ancilla vector which is filled with zeros.

OUTPUTS

The outputs of the system are one garbage vector of 8 bits, one sum vector of 4 bits and a Cout (Carry out) bit. Unfortunately, as can be seen, the garbage cost to realize this system is very high.

RESULTS

The project was simulated with the help of the Xilinx ISE 9.2 tool. Remember that the real inputs for this project were the 4 bits A and B and the 1 bit Cin (Carry In). The rest (K1 through K4) are only the ancilla bits and they need to remain always in zero. The reversible adder is being compared with the non-reversible adder and the floating point adder and the results are shown below in table 2

Table 2

S. No	.	Adder	Floating Point Adder	Reversible Adder
1	Number of Slice LUTs	3	552	12
2	Number used as Logic:	3	552	12
3	Number with an unused Flip Flop	3	223	12
4	Number of Bit Slices used:	0	894	0
5	Number of bonded IOBs:	4	199	26

CONCLUSIONS

We have designed efficient reversible adder using a novel reversible Peres gate. The proposed reversible adder designs are shown better than the existing one in literature in terms of number of LUT's and IBO's The proposed work shows the comparative study of reversible logic adder with the floating point adder and the full adder , the design of a specific reversible gate for a particular function can be very much beneficial. This can help in achieving the reductions in number of reversible gates, garbage outputs and quantum cost, and can be considered an important contribution of this work to the reversible logic community along with the design of efficient binary adders.

REFERENCES

1. Landauer, R., 1961. Irreversibility and heat generation in the computing process. IBM J. Res. Develop., 5: 183-191.
2. Md. Selim Al Mamun, Indrani Mandal, Uzzal Kumar Prodhan, International Journal of Science and Technology Volume 1 No. 10, October, 2012 “Quantum Cost Optimization for Reversible Carry Skip BCD Adder”.
3. Keyes, R.W. and R. Landauer, 1970. Minimal energy dissipation in logic. IBM J. Res. Develop., pp: 152-157.
4. Bennett, C.H., 1973. Logical reversibility of computation. IBM J. Res. Develop., 17: 525-532.
5. Bennett, C.H., 1988. Notes on the history of reversible computation. IBM J. Res. Develop., 32: 16-23.
6. Perkowski, M., L. Jozwiak, P. Kerntopf, A. Mishchenko and A. Al-Rabadi et al., 2001. A general decomposition for reversible logic. In: 5th Intl. Red-Muller Workshop, pp: 119-138.
7. Saiful Islam and Rafiqul Islam., 2005. Minimization of Reversible Adder Circuits. Asian Journal of Information Technology 4 (12): 1146-1151.
8. Peres, A. 1985. Reversible logic and quantum computers. Physical Review A, 32: 3266-3276. consecutively within brackets

9. A. D. Vos and Y. Van Rentergem, "Power consumption in reversible logic addressed by a ramp voltage", Proc. of the 15th Intl. Workshop Patmos 2005, Lecture Notes of Computer Science, vol. 3728, pp. 207-216, Springer-Verlag, Oct 2005.

10. E. Fredkin, T Toffoli, "Conservative Logic", Int. J. Theor. Phys, vol. 21, no. 3–4, pp. 219–253, 1982 [10] T. Toffoli, "Reversible Computing", Tech memo MIT/LCS/TM-151, MIT Lab for Computer Science (1980).

11. Ange anisotropy," in Magnetism, vol. III, G. T. Rado and H. Suhl, Eds. New York: Academic, 1963, pp. 271–350.